	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	2122	estimat$3 near5 (net or path)	USPAT	2002/01/17 06:30
2	BRS	L2	78	1 same (rc or resistance or capacitance)	USPAT	2002/01/17 06:31
3	BRS	L3	16	2 same (combin$3 or attach$4 or join$3 or add$3)	USPAT	2002/01/17 06:32
4	BRS	L4	46	2 and 716/$.ccls.	USPAT	2002/01/17 06:37
5	BRS	L7	0	5 and floorplan	USPAT	2002/01/17 06:32
6	BRS	L6	3	4 and floorplan	USPAT	2002/01/17 06:32
7	BRS	L5	10	3 and 716/$.ccls.	USPAT	2002/01/17 06:34
8	BRS	L8	36	4 not 5	USPAT	2002/01/17 07:07

	Type	Hits	Search Text	DBs	Time Stamp
15	BRS	2888	716/$.ccls.	USPAT	2002/01/15 08:35
16	BRS	4	generat$3 with (multi$3 or plural$3) with floorplan$	USPAT	2002/01/15 08:43
17	BRS	4	716/$.ccls. and (generat$3 with (multi$3 or plural$3) with floorplan$2)	USPAT	2002/01/15 08:35
18	BRS	5	select$3 with (multi$3 or plural$3) with floorplan$2	USPAT	2002/01/15 08:49
19	BRS	3	(choose or cho$4) with (multi$3 or plural$3) with floorplan$2	USPAT	2002/01/15 08:47
20	BRS	18	(select$3 or choose or chosen or chosing) with floorplan$2	USPAT	2002/01/15 08:50
21	BRS	13	((select$3 or choose or chosen or chosing) with floorplan$2) not ((716/$.ccls. and (generat$3 with (multi$3 or plural$3) with floorplan$2)) (select$3 with (multi$3 or plural$3) with floorplan$2) ((choose or cho$4) with (multi$3 or plural$3) with	USPAT	2002/01/15 08:50
22	BRS	4	716/$.ccls. and (((select$3 or choose or chosen or chosing) with floorplan$2) not ((716/$.ccls. and (generat$3 with (multi$3 or plural$3) with floorplan$2)) (select$3 with (multi$3 or plural$3) with floorplan$2) ((choose or cho$4) with (multi$3 or plural$3) with floorplan$2)))	USPAT	2002/01/15 08:50
23	BRS	57	("716/.CCLS.) and (floorplan$3 with (block$2 or module$2 or macro$2 or unit$2 or cell$2))	USPAT	2002/01/15 14:50
24	BRS	27	(("716/.CCLS.) and (floorplan$3 with (block$2 or module$2 or macro$2 or unit$2 or cell$2))) and ((rc or resistance or capacitance) and (rout$3 or	USPAT	2002/01/15 14:52
25	BRS	22	(("716/.CCLS.) and (floorplan$3 with (block$2 or module$2 or macro$2 or unit$2 or cell$2))) and ((rc or resistance or capacitance) same (rout$3 or path$2))	USPAT	2002/01/15 15:18
26	BRS	162	716/10.ccls.	USPAT	2002/01/15 15:19
27	BRS	58793	(rc or (resistance with capacitance))	USPAT	2002/01/16 09:05
28	BRS	23	((rc or (resistance with capacitance))) with netlist	USPAT	2002/01/16 09:50

	Type	Hits	Search Text	DBs	Time Stamp
29	BRS	1652	estimat$3 with (signal or wir$3 or path or net) with block$2	USPAT	2002/01/16 09:53
30	BRS	2	(estimat$3 with (signal or wir$3 or path or net) with block$2) same (model and (rc or resistance and capacitance))	USPAT	2002/01/16 10:16
31	BRS	23	(("716/8").CCLS.) and (floorplan$3 with (block$2 or module$2 or macro$2 or unit$2 or cell$2))	USPAT	2002/01/16 10:25

DOCUMENT-IDENTIFIER: US 6117182 A
TITLE: Optimum buffer placement for noise avoidance

DEPR:
The present invention accepts data consisting of routed conductors which form a tree topology. A circuit model is generally utilized. It is preferred that the circuit data has been defined or that an initial "Steiner estimation" of the net to be processed is available. A Steiner estimation is created by a specific design tool which utilizes known locations of the source and the sinks and creates an interconnected RC network. Steiner estimation design tools are well known by those having skill in the art.

CCOR:
716/8

CCXR:
716/17

DOCUMENT-IDENTIFIER: US 6099578 A
TITLE: Method of estimating wire length including correction and summation of estimated wire length of every pin pair

BSPR:
Preferably, the method may further include the step of calculating resistance value of the pin pair based on the estimated wire length of the pin pair, the step of calculating capacitance value of the net based on the estimated wire length of the net, and the step of calculating delay time when a signal passes through a signal path on the net, based on the resistance value of the pin pair and the capacitance value of the net.

BSPR:
According to the present invention, resistance value of the pin pair is calculated based on the highly precise estimated wire length of the pin pair, and capacitance value of the net is calculated based on the highly precise estimated wire length of the net. Therefore, the resistance value of the pin pair and the capacitance value of the net are both of high precision. The delay time when a signal passes through a signal path on the net is calculated based on the highly precise resistance value of the pin pair and the highly precise capacitance value of the net. This allows highly precise estimation of the signal delay time.

BSPR:
Preferably, the method may further include the step of calculating capacitance value of the net based on the estimated wire length of the net, and the step of calculating power consumption of the net based on the capacitance value of the net and a prescribed signal change rate of the net.

BSPR:
According to the present invention, the capacitance value of the net is estimated with high precision based on the estimated wire length of the net estimated with high precision. Power consumption of the net is estimated based on the highly precise capacitance value of the net. This allows highly precise estimation of power consumption of the net.

DEPR:
Capacitance value of the net to which the pin pairs belong is estimated (ST29). The capacitance value of the net is obtained by multiplying the estimated wire length of the net by an wiring capacitance value per unit wiring length determined by the design rule.

DEPR:
By timing verifying apparatus 200 described above, the resistance value of the pin pair can be estimated with precision based on the highly precise estimated wire lengths of the pin pairs. Further, the capacitance value of the net can be estimated with high precision based on the highly precise estimated wire length of the net. The highly precise resistance value of the pin pairs

and
the capacitance value of the net allows highly precise estimation of signal
delay, and allows highly precise timing verification.

DEPR:
Capacitance value of the virtual wiring of each net is estimated (ST35). The
capacitance value of the net is obtained by multiplying estimated wire length
of the net by signal change rate of the net obtained from the result of logic
simulation or the like, and further multiplying the result by a coefficient
determined by design rule.

DEPR:
Power consumption of each net is estimated (ST36). Power consumption of the
net is obtained, for example, by multiplying the capacitance value of the net
by the signal change rate of the net, and multiplying the result by a coefficient determined by the design rule.

DEPR:
By the power consumption estimating apparatus 300 described above, the
capacitance value of the net can be estimated with high precision based on
highly precise estimated wire length of the net. Accordingly, power consumption of the net can be estimated with high precision using the highly
precise capacitance value of the net and the signal change rate of the net.

CLPV:
based on the estimated wire length of said net, calculating capacitance value

of said net; and

CLPV:
based on the estimated wire length of said net, calculating capacitance value
of said net; and

CCOR:
716/4

CCXR:
716/12

DOCUMENT-IDENTIFIER: US 5475607 A
TITLE: Method of target generation for multilevel hierarchical circuit designs

CLPR:
6. A method according to claim 2, wherein, if a net does not have a known path, and the net has end-points that are not fixed in location, and the net does not have a specified net measure, then step (e) comprises determining an estimated average connection length for the net and determining net measure for each source/sink pair of the net using estimated resistive-capacitance delay for said estimated average connection length for determining net measure of the net.

CCOR:
716/10

CCXR:
716/6